CLAIMS

We claim:

1. ~~A method for maintaining translation lookaside buffer ("TLB") coherency in a~~ computer system having a plurality of processors, each of said processors having an associated TLB for storing an address translation data, the system having a main communication network coupled to the plurality of processors, said method comprising:

accessing a virtual address in said associated TLB and locating a corresponding associated physical address;

sending a TLB message from one of said plurality of processors to said main communication network if: (1) inputting a first entry into said associated TLB when said corresponding associated physical address is not located; (2) moving a second entry within said corresponding associated physical address to another location within said computer system; or (3) removing said second entry; and

sending said TLB message from said main communication network to said ~~plurality of processors.~~

2. The method of claim 1 wherein said TLB message further comprises:

a request for a read access to said first entry to add said address translation data into said associated TLB.

3. The method of claim 1 wherein said TLB message further comprises:

a request for a write access to said second entry and to invalidate all copies of said second entry in each of said associated TLB in said plurality of processors.

4. The method of claim 1 further comprising:

comparing said first entry with said address translation data in said associated TLB and informing said associated TLB if said first entry affects said address data stored therein.

5. The method of claim 4 further comprising adding said address translation data in said first entry into said associated TLB in each of said plurality of processors.

6. The method of claim 1 further comprising:

comparing said second entry with said address data in said associated TLB and informing said associated TLB if said second entry affects said address data stored therein.

7. The method of claim 6 further comprising invalidating said address translation data in said second entry in said associated TLB in each of said plurality of processors.

8. A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform a method for maintaining TLB coherency in a computer system including a plurality of processors each having an associated TLB for storing address data and a main central processing unit coupled to the plurality of processors, said method comprising:

accessing a virtual address in said associated TLB and locating a corresponding associated physical address;

sending a TLB message from one of said plurality of processors to said main communication network if: (1) inputting a first entry into said associated TLB when said corresponding associated physical address is not located; (2) moving a second entry within said corresponding associated physical address to another location within said computer system; or (3) removing said second entry; and

sending said TLB message from said main communication network to said plurality of processors.

9. An electronic data processing apparatus, comprising:

a plurality of processors;

a plurality of TLBs, each of said plurality of TLBs connected to and associated with a respective processor of said plurality of processors;

an interconnect network having a plurality of independent paths, said plurality of processors distributed among said plurality of independent paths with each said processor connecting to one of said plurality of independent paths; and

a TLB message generator having an accessed data address and a TLB message ~~transmitted on said plurality of independent paths.~~

Sub B4

10. The apparatus of claim 9 wherein said TLB message further comprises:

a read access message if said accessed data address is inputted into said associated TLB.

11. The apparatus of claim 9 wherein said TLB message further comprises:

a write access message if said accessed data address invalidates said address translation data in said associated TLB.

Sub A3

12. ~~A system for TLB coherency in a computer system, comprising:~~

a plurality of processors;

a plurality of TLB, each of said plurality of TLB is connected to and associated with a respective processor of said plurality of processors;

an interconnect network having a plurality of independent paths, said plurality of processors is distributed among said plurality of independent paths with each processor and its associated TLB connecting to one of said plurality of independent paths;

performing an access to a data address from its said associated TLB;

a TLB message generator having a TLB message; and

transmitting said TLB message and said access data to a main communication network.

13. The system of claim 12 further comprising transmitting said TLB message and said access data on said plurality of independent paths and comparing said accessed data address with an address translation data of the information stored in each of said plurality of TLB and said TLB message will inform each of said plurality of TLB if said access data address affects data stored therein.

14. The system of claim 12 further comprising adding said access data address into said associated TLB in each of said plurality of processors.

15. The system of claim 12 further comprising invalidating said address translation data in said associated TLB in each of said plurality of processors.

16. The system of claim 12 further comprising moving said address translation data in said associated TLB in each of said plurality of processors to another part of the computer system.

17. The system of claim 12 wherein the TLB message generator further comprises:

a read access message if said accessed data address is inputted into said associated TLB.

18. The system of claim 12 wherein the TLB message generator further comprises:

a write access message if said accessed data invalidates said address translation ~~data in said associated TLB.~~

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